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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,280	01/22/2002	Atsushi Shimbo	04284.0856	7579
7590	11/18/2004			EXAMINER DO, CHAT C
Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P. 1300 I Street, N.W. Washington, DC 20005-3315			ART UNIT 2124	PAPER NUMBER

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/051,280	SHIMBO, ATSUSHI
	Examiner	Art Unit
	Chat C. Do	2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 1/22/02; 3/22/02; 10/1/02; 11/04/02.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-20 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s):

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3/22/02;11/4/02.
4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: ____.

DETAILED ACTION

Claim Objections

1. Claims 3-4 and 5-6 are objected to because of the following informalities:

Re claims 3-4 and 5-6, these claims are very similar to claims 1-2 respectively, except the limitations are cited not in order as original claims 1-2 and wording slightly different but same meaning. The applicant is advised either to cancel these claims to avoid duplication or modified these claims to clearly distinguish them from the original claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, the limitation “the basis of a residue number system” in line 2 lacks an antecedence basis. For examination purposes, the examiner considers the limitation as “a basis of a residue number system”. Claims 3, 5, 10, 12, 14, and 16 have same rejection.

Thus, claims 2, 4, 6-9, 11, 13, 15, and 17-20 are also rejected for being dependent upon the rejected based claims 1, 3, 5, 10, 12, 14, and 16 respectively.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-8 and 10-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kenneth et al. ("The Use of Residue Number Systems in the Design of Finite Impulse Response Digital Filters").

Re claim 1, Kenneth et al. disclose in Figures 2 and 8 a modular arithmetic apparatus (abstract in page 191, lines 5-8) for performing an arithmetic operation of an integer (equation 4 in page 193) on the basis of a residue number system (RNS), comprising: an input unit configured to input data (e.g. input data as $u(n)/x(n)$) included in modulus p (e.g. page 192 right column under Residue Number Systems section lines 15-16) and to output an arithmetic result (e.g. Figure 8 $y(n)$), a plurality of operation units (e.g. $F_1(j)+Mod_p$ adder+latch as 1 unit in Figure 2) configured to perform residue operations in parallel (e.g. in Figure 2 as seen four units operate in parallel) to obtain the arithmetic result (e.g. Figure 8 $y(n)$), each operation unit (e.g. $F_1(j)+Mod_p$ adder+latch as 1 unit in Figure 2) having a storage unit (e.g. $F_1(j)$ in Figure 2 and last paragraph in page 193 right column) which stores at least a portion of a plurality of base parameter sets,

each one of base parameter sets containing a different number of base parameters (e.g. last three lines in page 193 right column), and a selection unit (e.g. all the AND gate in Figure 2 for selecting the appropriate ROM) for configured to select one base parameter set in the plurality of base parameter sets according to the modulus p input from input unit (e.g. equations 8 and 9 in page 194).

Re claim 2, Kenneth et al. further disclose in Figures 2 and 8 a selection unit selects a minimum base parameter set from base parameter sets, for which a product of base elements is larger than the modulus p (e.g. equation 6 in page 193 right column).

Re claim 3, Kenneth et al. disclose in Figures 2 and 8 a modular arithmetic apparatus (abstract in page 191, lines 5-8) for performing an arithmetic operation of an integer (equation 4 in page 193) on the basis of a residue number system (RNS), comprising: an input/output unit configured to input data (e.g. input data as $u(n)/x(n)$) included in modulus p (e.g. page 192 right column under RNS section lines 15-16); a plurality of operation units (e.g. $F_1(j) + \text{Mod}_{p_1}\text{adder} + \text{latch}$ as 1 unit in Figure 2), each operation unit (e.g. Figure 8 $y(n)$), each operation unit (e.g. $F_1(j) + \text{Mod}_{p_1}\text{adder} + \text{latch}$ as 1 unit in Figure 2) having a storage unit which stores at least a portion of a plurality of base parameter sets, each one of base parameter sets containing a different number of base parameters, a selection unit (e.g. all the AND gate in Figure 2 for selecting the appropriate ROM) configured to select one base parameter set in the plurality of base parameter sets according to the modulus p input from input/output unit (e.g. input data as $u(n)/x(n)$); plurality of operation units configured to perform residue operations in parallel (e.g. in Figure 2 as seen four units operate in parallel) according to the selected

one base parameter set and to obtain an arithmetic result; and input/output unit configured to output the arithmetic result (e.g. Figure 8 as $y(n)$).

Re claim 4, it has limitations cited in claim 2. Thus, claim 4 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 5, Kenneth et al. disclose in Figures 2 and 8 a modular arithmetic apparatus (abstract in page 191, lines 5-8) for performing an arithmetic operation of an integer (equation 4 in page 193) on the basis of a residue number system (RNS), comprising: an input/output unit (e.g. input data as $u(n)/x(n)$) configured to input data included in modulus p (e.g. page 192 right column under RNS section lines 15-16) and to output an arithmetic result (e.g. Figure 8 as $y(n)$), a storage unit configured to store at least a portion of a plurality of base parameter sets (ROM for storing partial results), each base parameter set including a set of base parameters indicating base elements, each one of plurality of base parameter sets contains a different number of base parameters, and a base selection unit (e.g. all the AND gate in Figure 2 for selecting the appropriate ROM) configured to select one base parameter set in storage unit according to the modulus p input from input/output unit; and a plurality of arithmetic units (e.g. $F_1(j) + Mod_p$ adder+latch as 1 unit in Figure 2), configured to perform operations in parallel (e.g. in Figure 2 as seen four units operate in parallel) according to the selected one base parameter set to obtain the arithmetic result (e.g. Figure 8 as $y(n)$).

Re claim 6, it has limitations cited in claim 2. Thus, claim 6 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 7, Kenneth et al. further disclose in Figures 2 and 8 the numbers of the base parameters of each base parameter set in storage unit are multiples of the number of the arithmetic units, respectively (e.g. there are one ROM for each arithmetic units in Figure 2 and each of them contain a set of result as seen in page 193 right column. Thus, the total partial results must be a multiple of the number of the arithmetic units).

Re claim 8, it has limitations cited in claim 2. Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 10, it is a means limitations claim of claim 1. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 11, it has limitations cited in claim 2. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 12, Kenneth et al. disclose in Figures 2 and 8 a modular arithmetic apparatus (abstract in page 191, lines 5-8) for performing an arithmetic operation of an integer (equation 4 in page 193) on the basis of a residue number system (RNS), comprising: an input/output unit (e.g. input data as $u(n)/x(n)$) configured to input data included in modulus p (e.g. page 192 right column under Residue Number Systems section lines 15-16) and to output an arithmetic result (e.g. Figure 8 $y(n)$); a plurality of storage units (e.g. $F(\cdot)$ in Figure 2) configured to store at least a portion of a plurality of base parameter sets, each base parameter set including a set of base parameters indicating base elements, each one of plurality of base parameter sets contains a different number of base parameters (e.g. last three lines in page 193 right column) and, a base selection unit (e.g. all the AND gate in Figure 2 for selecting the appropriate ROM) configured to select

one base parameter set in storage units according to the modulus p input from input/output unit (e.g. equations 8 and 9 in page 194); and, a plurality of arithmetic units (e.g. $F_1(j) + \text{Mod}_p \text{adder} + \text{latch}$ as 1 unit in Figure 2) configured to perform operations in parallel according to the selected one base parameter set to obtain the arithmetic result (e.g. in Figure 2 as seen four units operate in parallel).

Re claim 13, it has limitations cited in claim 2. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 14, it is a method claim of claim 1. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 15, it is a method claim of claim 2. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 16, it is a method claim of claim 5. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 17, it is a method claim of claim 6. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 18, it is a method claim of claim 7. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 19, it is a method claim of claim 8. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Allowable Subject Matter

6. Claims 9 and 20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. U.S. Patent No. 5,077,793 to Falk et al. disclose a residue number encryption and decryption system.
- b. U.S. Patent No. 6,148,034 to Lipovski discloses an apparatus and method for determining video encoding motion compensation vectors.
- c. U.S. Patent No. 6,240,436 to McGregor discloses a high speed Montgomery value calculation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2124

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

November 15, 2004

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